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Electronic materials

All-inkjet-printed high-performance flexible MoS_2 and MoS_2-reduced graphene oxide field-effect transistors

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ABSTRACT

Two-dimensional (2D) materials have been utilized to design flexible field-effect transistors (FETs) with promising performance. However, flexible FETs still face challenges with poor switching features and ultra-low drive current. In this paper, a facile and repeatable large-area integration process is presented for inkjet-printed FETs with 2D materials active channels and PI films as gate dielectrics. The MoS_2 FETs reported here exhibit *n*-type channel feature with an outstanding average subthreshold swing of 75 mV/dec, an on-state/off-state current ratio of 10^4, and on-state current up to 10 μA at a power supply voltage of 3.0 V. Besides, MoS_2–rGO FETs also exhibit *n*-type semiconductor features with good electrical properties by the inkjet-printing technology.

Introduction

In recent years, two-dimensional (2D) van der Waals materials have attracted much attention in virtue of their significant potential for next-generation nano-electronic devices. Among these 2D materials, channels made of MoS_2 [1, 2], reduced graphene oxide (rGO) [3–5] and carbon nanotubes [6–8] have been used in field-effect transistors (FETs), due to their high mobility and optical properties. The MoS_2 bandgap varies with the number of layers (about 1.3 eV for multilayer MoS_2 and about 1.8 eV for monolayer MoS_2) [9–11]. Various techniques for the synthesis and integration of large-area ultrathin MoS_2 films were proposed including chemical vapor

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deposition (CVD) growth techniques [12, 13] and liquid-phase exfoliation [14–19]. Although CVD growth of 2D materials may result in high-quality nanoscale devices, this fabrication process needs reliable and rigorous clean conditions. Moreover, the transfer of CVD-grown monolayer or multilayer 2D materials to Si/SiO_2 substrates remains unreliable [20]. Liquid phase exfoliation can easily produce multilayer MoS_2 on a large scale, and it is conducive to prepare printable inks directly using dispersion obtained thereby.

Polyimide (PI) is a heat-resistant polymer material that has been utilized by several groups for surface integration with different inorganic/organic components [20–23]. Because of its unique characteristics, PI has been successfully applied in flexible sensors and PCB circuits, such as in high-density integration for information storage devices. The patterned electrode on PI is essential for these applications, which can be produced via traditional mask-based photolithography or digital printing technology [24–26]. However, there are many constraints in printing process, like particle size, ink concentration and nozzle clogging, and the surface deposited electrode film shows poor adhesion on PI substrate. Thus, Ag electrodes with high adhesion were prepared by in situ reduction on the surface of PI substrate.

Up to now, 2D materials integrated on flexible substrate to fabricate flexible FETs need complex procedure and is still lack of thorough research. This makes high integration and high-performance flexible FETs still face numerous challenges such as: (1) The typical subthreshold swing (*SS*) and drive current of back-gate 2D materials channel FETs is poorer and smaller than that of the standard silicon transistors. (2) Multi-step procedure and low-efficiency fabrication should be improved to increase device integration. (3) The interconnection of 2D materials nanosheets should be easy to obtain, which is a key point for efficiency and reliability of flexible devices.

Therefore, to reduce production complexity and address these challenges, we directly employed a flexible PI substrate as a gate dielectric layer with the relative permittivity of 3.5. Moreover, silver on one side of this dielectric could serve as a back-gate and, on the other side, can be patterned as source and drain contact electrodes by inkjet printing combined with in situ reduction. FETs channels of MoS_2 and MoS_2 mixed with reduced graphene oxide (rGO) were fabricated by printing technique to compare FETs electrical performance. Finally, the annealing process of MoS_2 and MoS_2–rGO FETs at 90 °C was needed in order to remove residual contaminations. As a result, the integration challenges mentioned above were successfully overcome, making large-area and reliable FETs possible.

Experimental

Materials

The PI film (thickness: 125 μm) was manufactured by Jinteng plastic Co. Ltd. Ethanol, sodium hydroxide, hydrogen peroxide, silver nitrate, MoS_2 powder, polyvinylpyrrolidone (PVP), and ammonium hydroxide were purchased from Nanjing Daoning chemical reagent Co. Ltd. All commercially available chemicals were utilized without further purification unless otherwise indicated. MoS_2 powder is ordered from Huajing Powdery Material Science & Technological Co. Ltd. Bulk nanosheet sizes range from 12 to 16 μm, purity is 99.9% (acid-insoluble substance: 0.04%, SiO_2: 0.02%, CuO: 0.01%, MoO_3: 0.03%).

Ink preparation

The MoS_2 ink used for printing doped with PVP, because researches have indicated that under the van der Waals force, it is difficult to disperse 2D materials which will have an adverse effect on the electrical and chemical properties. However, when the hydrophilic PVP can adsorb the surface of the MoS_2, the dissolution of the polymer chain impels the MoS_2 to disperse into the solution. The dispersibility of MoS_2 could be improved by PVP and MoS_2 inks were obtained by liquid-phase exfoliation. Ethanol (20 mL) and deionized water (20 mL) were put in a sealed container mixed with PVP (80 mg), MoS_2 (400 mg), and sonicated at 27 °C for 48 h. The resultant suspension was centrifuged at 7500 rpm for 15 min to sediment thick nanosheets, while the supernatant was obtained. Similarly, MoS_2–rGO dispersion was obtained by extra addition of rGO (40 mg) before sonication. Finally, a stable MoS_2 ink (2.13 mg/mL after ethanol evaporation) and a stable MoS_2–rGO ink (0.71 mg/mL) were prepared for printing, respectively. The final viscosity and surface tension of formulated inks are shown in Fig. S1.

Surface modification on PI substrate

The PI substrate first needed to be cleaned by plenty of deionized water and ultrasonic washing in deionized water and ethanol for 15 min. Afterward, the substrate was dried under nitrogen flow, immersed in 6 M NaOH solution at 40 °C for 2 h and then rinsed with copious deionized water. Alkaline treatment of PI film surface may generate carboxylic acid groups and amide bonds. After cleaning with deionized water, the modified PI substrate was immersed in aqueous silver–ammonia solution (0.4 M $AgNO_3$) for 20 min at room temperature following a previous report [27]. Finally, the PI film was washed with deionized water. Besides, the carbon ink and preparation process are utilized directly from the EPSON-L310. The low-cost carbon ink could be printed on the alkaline treatment of PI film surface directly after anneal at 90 °C as described in. The purpose is to reinforce adhesive force between the silver layer and PI, and then dried mask between electrodes could be easily removed through bending and could thermo-solidify and print the electrode patterns. So the carbon ink is not necessary to be special prepared.

Inkjet printing and electrode patterning

A redesigned commercial printer Epson-L310 was used to print MoS_2, MoS_2–rGO inks, and carbon mask. We redefine the "color cartridge" to print the corresponding inks, the black cartridge is still carbon powder that is used to print carbon mask in Fig. 1. Patterned source and drain electrodes were formed by the selective reduction of Ag^+ ions in hydrogen peroxide (30%) for 5 min. The distance between the two electrodes acted as the channel length. Unnecessary silver reduction on the PI surface was prevented in predefined regions by printed carbon acting as a mask. Then the source/drain electrodes array was obtained on one side of PI film. And the back-gate electrode was formed on the other side of PI film without printed carbon mask pattern. After that, the resulting sample was cleaned in deionized water and the printed carbon mask on channel was removed by reduction swelling reaction. Finally, MoS_2 and MoS_2–rGO active layer with about 100 μm channel length were formed by printing, and the channel width can be defined to 1000 μm.

Characterization

The optical microscope images were taken by Keyence VHX-500F Digital Microscope. FEI EDAX Genesis and Tecai G2 F20 S-Twin TMP are used for scanning electron microscopy (SEM) and transmission electron microscopy (TEM) analyses, respectively. The transfer and output characteristics of FETs were determined by an Agilent B1500a.

Results and discussion

Figure 1 shows the fabrication process of the flexible MoS_2 FETs and MoS_2–rGO FETs. The 2D material layer, back-gate, and source/drain electrodes are shown here to ensure better understanding of the printing technology.

Step 1: PI film (Fig. 2a) was chemically treated in a 6 M sodium hydroxide solution (2 h at 40 °C) to develop carboxyl groups at both sides and then cleaned with plenty of deionized water.

Step 2: Ag ions (Fig. 2b) were bound with carboxyl groups by substituting Na^+ ions through immersing surface-treated PI film into 0.4 M silver nitrate solution for 20 min at 27 °C.

Step 3: The masking technique specifically showing in this work is a facile method to design MoS_2 and MoS_2–rGO FETs. The carbon mask was produced by inkjet printing on one side of the PI film (Fig. 2c). To prevent the line edge roughness (LER) effects, the carbon powder must be solidified in this step at 180 °C for 3 min.

Step 4: Silver electrodes were formed via reduction reaction in alkaline hydrogen peroxide solution for 20 min at room temperature (Fig. 2d). Carbon powder prevents silver ions reduction so that the uncovered region would allow silver reduction to form source/drain and back-gate contacts. The sample was then placed in oven to crystallize reduced silver atoms at 180 °C for 3 min. Silver electrodes with low square resistance were achieved, ensuring good ohmic contact with 2D materials.

Step 5: The critical process is to remove the carbon powder between source/drain electrodes (Fig. 2e). The carbon powder could be easily removed by the silver reduction swelling reaction in 30% hydrogen peroxide solution for 5 min. There are four transistors in the basic cells that can be distinctly seen in the enlarged illustration, and the MoS_2 or MoS_2–rGO

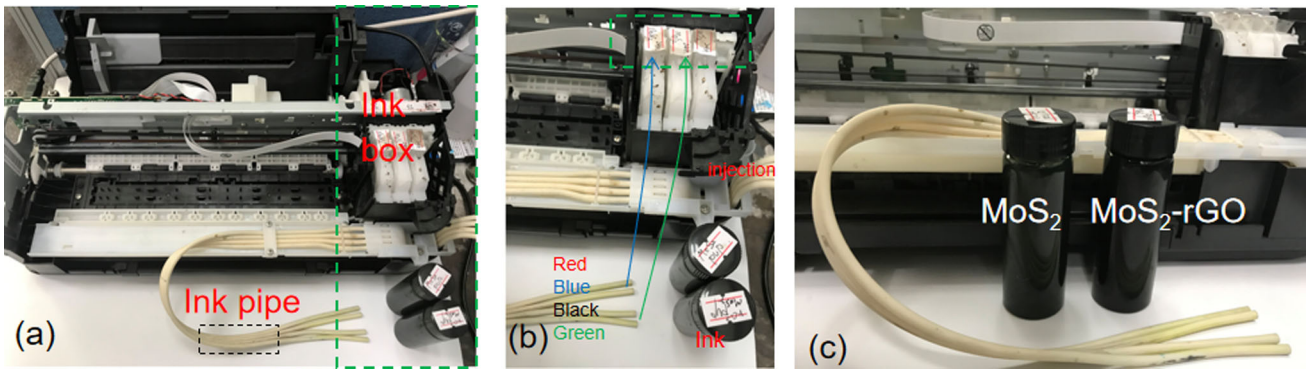

Figure 1 **a** A redesigned commercial printer Epson-L310, **b** ink pipes and cartridges and **c** bottled inks.

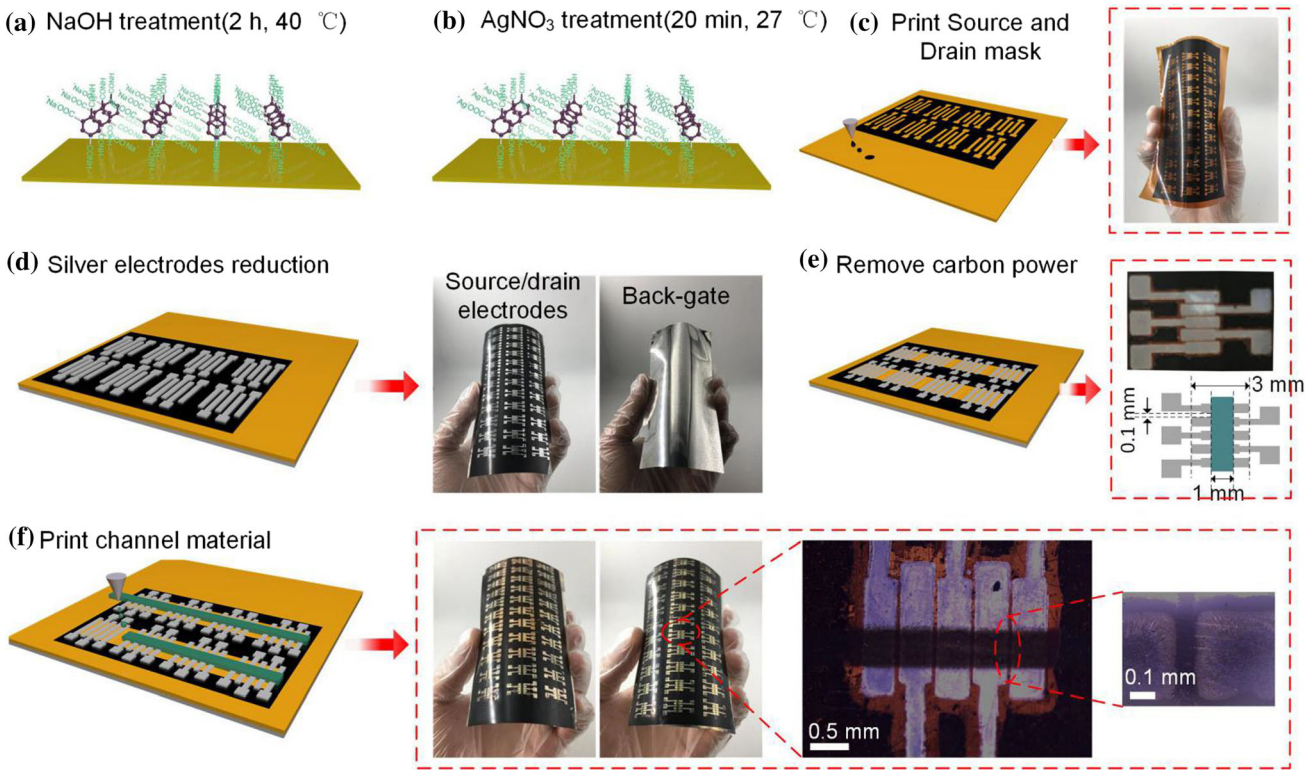

Figure 2 Schematic of the all-inkjet-printed FETs with PI as gate dielectric layer. The process **a** step 1: chemically disposed PI using sodium hydroxide (NaOH) to form sodium ion adsorption layer, **b** step 2: silver ion exchange with sodium ion, **c** step 3: printing source and drain mask, **d** step 4: silver reduction to form bottom gate, source and drain electrodes, **e** step 5: removing the carbon between source and drain, **f** step 6: printing MoS_2 and MoS_2–rGO FETs channel.

channels could be deposited onto the surface of the source and drain electrodes. Crucial parameters of the silver electrodes within the printed patterns were recorded. The width and the length of the channel were 1000 μm and 100 μm, respectively, and the silver pads were used for the contact probes to simplify electrical testing.

Step 6: To form a charge channel between source and drain electrodes, it is necessary to reprint channel materials (Fig. S2). The MoS_2 and the MoS_2–rGO inks meet the requirement to achieve a stable printing process with the inkjet printer employed in electrodes array. The purpose of repetitive printing is to ensure that small nanosheets are connected to each other as an integral transistor channel. This was achieved by printing each channel 20 times, enhancing the inter-nanosheets connectivity within channel. The channel length was optimized down to 100 μm controlled by

the distance between the source and the drain electrodes. The channel is shown in a zoomed-in optical microscope image to reveal the details between electrodes. Ultimately, these uniform MoS_2 and MoS_2–rGO channels could be obtained after evaporation for 30 min at 90 °C. The last annealing process removes solvents from the channel. The FETs were made of a single transistor with channel length and width of 100 μm and 1000 μm, respectively, as shown in Fig. 2f.

In order to obtain further information about MoS_2–rGO mixture inks, TEM images were obtained after 3 h sonication, as shown in Fig. 3a. rGO and MoS_2 nanosheets overlapping was observed. The magnified image in Fig. 2b further shows that rGO and MoS_2 nanosheets have a multilayer structure. In addition, the high-resolution TEM (HRTEM) image (Fig. 3c) for the white rectangular region marked in Fig. 3b confirms the overlapping and well-defined crystalline structures of MoS_2 and amorphous rGO by distinguishable lattice fringes. The corresponding selected area electron diffraction (SAED) image clearly shows diffraction spots representing the overlap of crystalline MoS_2 and amorphous rGO, as shown in Fig. 3d. Multilayer MoS_2 and few-layer rGO after 24 h sonication were revealed by TEM and the corresponding EDS elemental mapping in Fig. 3e. After 48 h liquid-phase sonication exfoliation, the lateral size of MoS_2 nanosheets decreased further as shown in Fig. 3f, and reduced layers were obtained from more transparency of TEM images. This few-layer thickness promotes charge-carrier transport among different layers.

Direct observation of MoS_2–rGO and MoS_2 FETs was performed by SEM, and the results are shown in Fig. 4a, d, respectively. The inkjet-printed channel consists of many 2D-materials networks because MoS_2 or rGO could be stacked together. Zoomed-in SEM images in Fig. 4b, e show that our inkjet process allows obtaining the ultrashort MoS_2–rGO and MoS_2 FETs channel lengths down to 100 μm. The stack structure of these stratified MoS_2–rGO and MoS_2 nanosheets was deposited on silver wires. The scanning widows marked the regions used in the channel cross-section analysis in Fig. 4c, f. According to the cross section, a continuous film of MoS_2–rGO or MoS_2 was formed on PI substrate, which suggest that the interconnected network of MoS_2 nanosheets form in transistor channel with an effective channel thickness of 1–1.5 μm. The gate electric field only influences

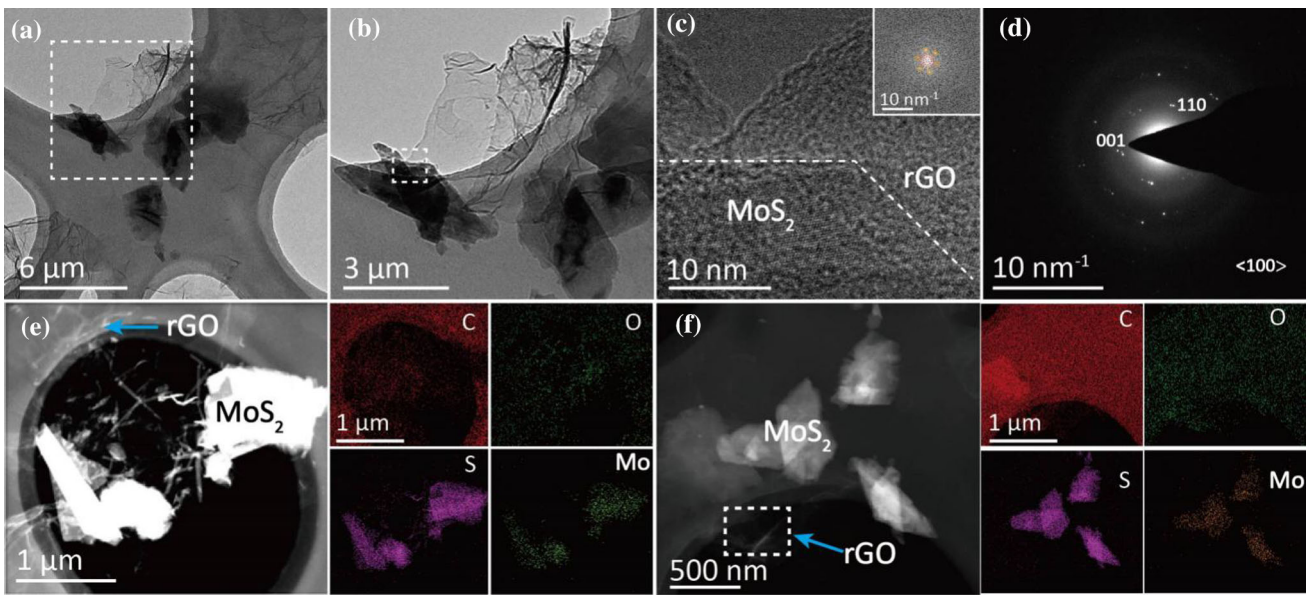

Figure 3 **a** TEM image for 3 h sonication showing MoS_2 nanoflakes (typical size is about 3 μm) and rGO, **b** Enlarged view of the areas marked with the white line in (**a**), **c** HRTEM image of MoS_2–rGO composite; the inset shows the corresponding FFT of MoS_2–rGO composite pattern, the brown solid circles represent MoS_2, and the dotted red circles represent rGO, **d** SAED image of the edge of the MoS_2–rGO nano crystallites, **e** TEM image of MoS_2–rGO nanoflakes (typical size of ~ 1 μm) after 24 h sonication and the corresponding EDS elemental mapping, **f** TEM image of MoS_2–rGO nanoflakes (typical size of ~ 0.5 μm) after 48 h sonication and the corresponding EDS elemental mapping. C and O arise from rGO, Mo and S arise from MoS_2 for every EDS elemental mapping.

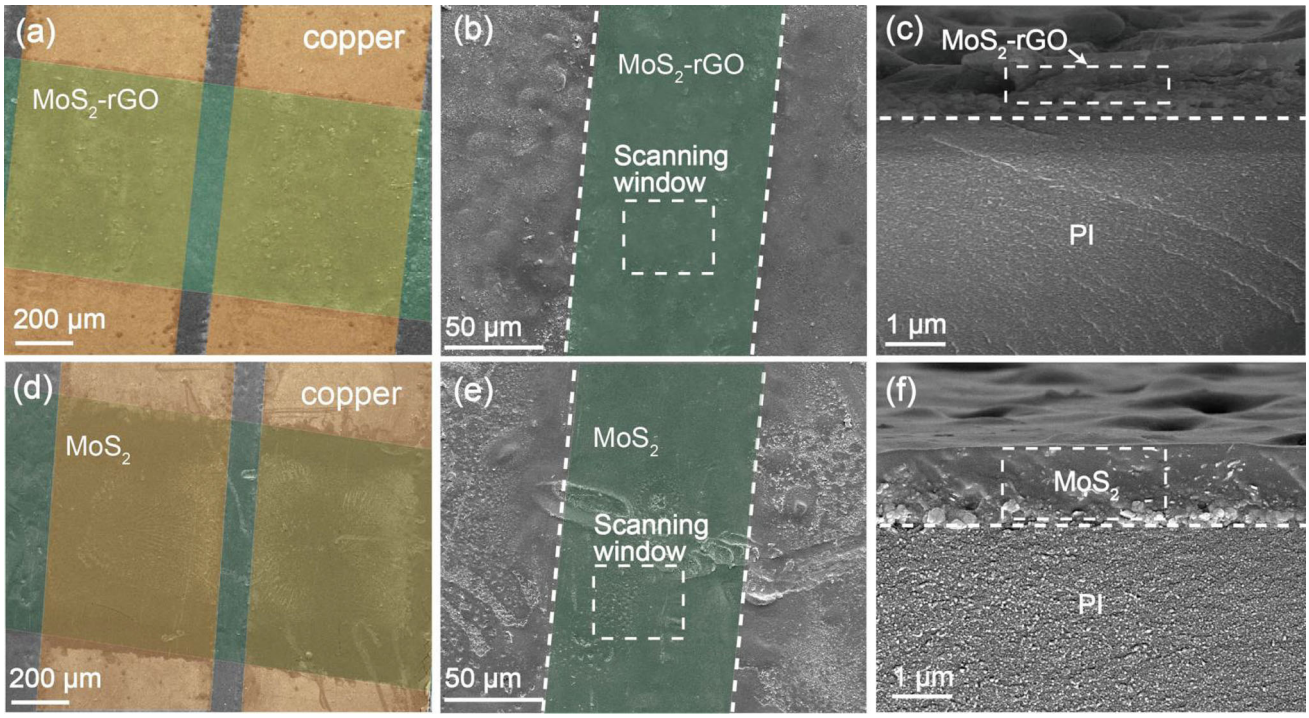

Figure 4 Top view SEM images of **a** MoS_2–rGO and **d** MoS_2 transistors. Top view SEM image of **b** MoS_2–rGO material and **e** MoS_2 material between source and drain electrodes. Cross-sections of **c** MoS_2–rGO and **f** MoS_2 channels.

1–1.5 nm of the channel surface under the gate dielectric layer. As a result, the MoS_2 or MoS_2–rGO nanoflakes could make a complete inner connecting path after 20 printings at the channel/PI interface.

Strictly speaking, the MoS_2–rGO FETs and MoS_2 FETs are a kind of junctionless device. Figure 5a, d shows the side view of MoS_2–rGO and MoS_2 nanosheets transistor. The few-layer MoS_2–rGO and MoS_2 nanosheets were printed between electrodes, which results in an edge-type contact [28–35]. It is beneficial to reduce the ohmic resistance of metal–semiconductor (MS) contact system. The top view of the printed MoS_2–rGO channels are also shown in Fig. 5a, the MoS_2 crystals play a role in connectivity between rGO sheets, which is beneficial to the characteristic of FETs switching. The rGO size is notably larger than that of MoS_2 as shown in Fig. 3, which could make MoS_2 nanosheets wrap around rGO layers. On the other hand, repeated printing makes MoS_2 nanosheets string together in different networks. This is also illustrated by the top view of the printed MoS_2 channel schematically shown in Fig. 5d. Figure 5b, e shows the output characteristics obtained from the printed MoS_2–rGO and MoS_2 FETs with a sweeping drain voltage at three different gate voltages (2 V, 4 V, and 6 V). The output characteristics exhibit *n*-type gate modulation transistor. When a testing voltage is applied at the bottom gate, the gate to source voltage pulls down the energy band of the MoS_2–rGO channel and reduces the height of the Schottky barrier [36, 37] at the source/channel junction, then the *n*-type device switches to its on-state.

The excellent performance of the MoS_2–rGO or MoS_2 FETs can be explained in the following way: When the bottom-gate bias V_{BG} is lower than threshold voltage (V_{TH}), there is no carrier accumulation because the Schottky barrier of MS edge-type contact is large. If the MS barrier height is reduced due to the channel energy band modulation, then the carriers can injected from the valence band of the source to the conduction band or defect state band of the channel giving rise to a carrier injection current. The barrier height would decrease with a reduced dependence for increasing back-gate voltage V_{BG} (from 2 to 6 V). When V_{BG} reaches overdrive voltages, the lowest MoS_2 layer releases electrons forming an accumulation charge layer at the channel/PI interface. If V_{DS} is further increased, V_{DS} appears across the Schottky barrier at the source/channel junction and giving rising to the tunnelling current.

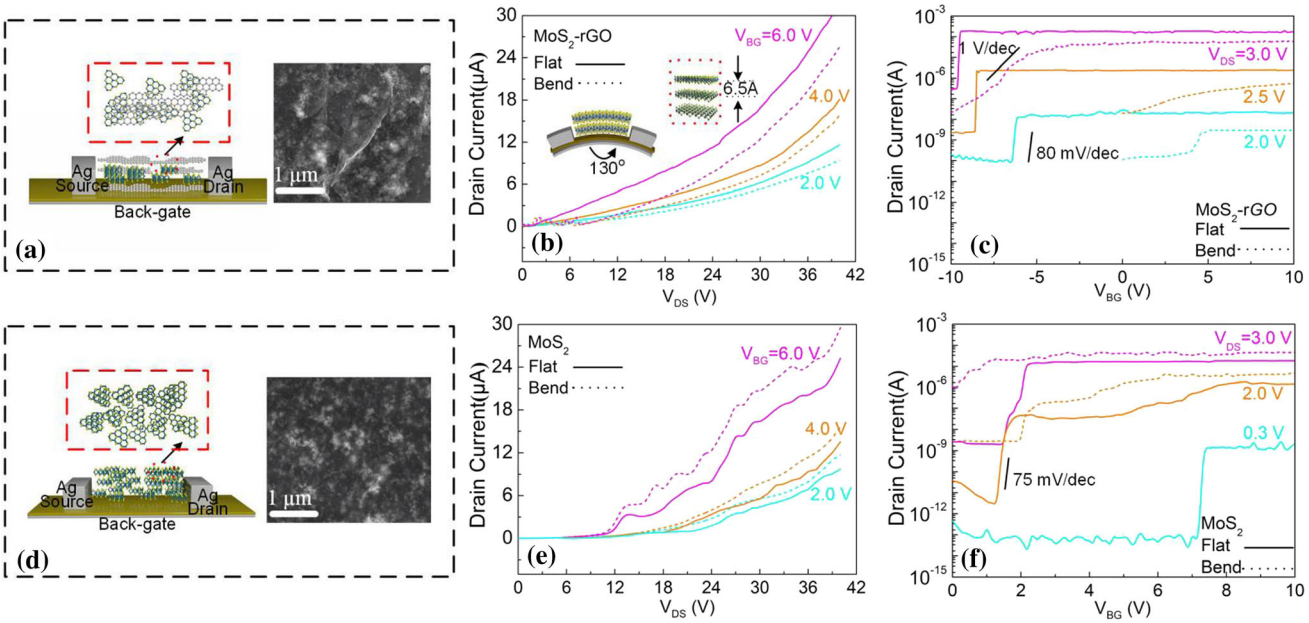

Figure 5 Electrical performances of the all-inkjet-printed and simulation FETs. Schematic illustrations of the electrical contact geometries in printed **a** MoS_2–rGO channel and SEM of the hybrid MoS_2 and rGO nanosheets, **d** MoS_2 channel and only MoS_2 nanosheets. The output characteristics of **b** MoS_2–rGO FETs and **e** MoS_2 FETs with channel width of 100 μm, V_{DS} is in the range of 0–40 V. Transfer characteristics of **c** width of MoS_2–rGO and **d** MoS_2 FETs with 1000 μm and channel length = 100 μm at different V_{DS}.

The effect from the lateral or vertical electric field and remote impurity scattering on the electron mobility cannot be neglected through defect-bound band edge states transport [38]. That is why the electron mobility would be limited for all-inkjet-printed 2D material transistors. It can be inferred that the electron concentration increases linearly at the interface of the lowest channel layer and PI with increasing V_{BG}. The top MoS_2–rGO layers start to supply electrons to reduce channel resistance at the surface of PI for higher back gate V_{BG} = 6 V. As a result, the drain current increases for different V_{BG} and a fixed V_{DS} in this region, which can be considered as the channel-resistance-limited region. The high concentration MoS_2 ink made an integrated MoS_2 network of pathways possible. Electron tunnelling appears at the Schottky barrier junction of the channel and the source for the MoS_2 FETs. The electron concentration on the PI substrate region uniformly increases for increasing V_{BG}. The electrons lateral tunneling effects contribute to FETs switch characteristic (75 mV/dec).

As the effective transport paths of the carriers had been strongly reduced, and thus the output current of the MoS_2–rGO transistor would decrease as evidenced in Fig. 5b. The output characteristics, shown in Fig. 5e, nevertheless, show a different behavior for the MoS_2 transistor. Biaxial tension by local mechanical stress has been observed to be more suitable for the band structure engineering with small bending angle and enhanced carrier mobility [39]. The strain source of the channel by mechanical stress between two-dimensional material leads to a large tensile stress and driving current improvement. As the lattice spacing of the surface group of PI mismatch with the MoS_2 nanosheets, and the bending angle of the bottom MoS_2 layer is also larger than that of the PI substrate, the carrier mobility would change once the PI was bent. And then the drive current would decrease after bending. This can be explained if the bending angle is large enough to break the MoS_2 nanosheets network pathway leading to a significant mobility reduction. Ultimately, a right bending angle of 50° for the MoS_2 FETs was found so that the drain current could be maximal after 200 bending experiments cycling.

For the transfer characteristics of printed transistors, Fig. 5c shows the effect of gate voltage on the transfer characteristics of the MoS_2–rGO FETs. A change in V_{DS} results in a linear shift of the transfer

characteristics, including a linear shift of V_{TH} and a linear increase of the off-state current (I_{OFF}). The threshold voltage shift can be explained by the non-uniformity of electron concentration at the accumulation layer for different V_{DS}. The position of electron concentration changed because of transformation of the charge network pathway and vertical/horizontal electric field. For MoS_2–rGO FETs, the *SS* shows poor feature (almost 1 V/dec after being bent) and the I_{ON} (100 μA at V_{DS} = 3.0 V and V_{BG} = 10.0 V) decrease with the same V_{DS} after bending in Fig. 5c, as the carriers transport pathway have been changed or even tensile failure occurred, compared with previous reports [40]. The SS characteristics of MoS_2–rGO FETs were improved dramatically due to existence of MoS_2 crystal, which is promising to obtain high electron mobility at room temperature.

In order to elucidate the effects of MoS_2 ink on the conduction mechanism, the transfer characteristics of all-inkjet-printed MoS_2 FETs were recorded as shown in Fig. 5f. The subthreshold swing of the MoS_2 FETs was close to the theoretical value of 60 mV/dec. The threshold voltage drift (∼ 0.2 V) is smaller than that of the MoS_2–rGO FETs. The channel width increases the on-state current, and the thickness of it also changes the threshold voltage. The transfer current (channel width of 1000 μm) is not seven times of the output current (channel width of 100 μm). This result can be explained as due to the presence of PVP residues in inks that is favorable to formation of a tight network pathway made of MoS_2 nanosheets. The I_{ON}/I_{OFF} ratio reaches nearly 10^4 at V_{DS} = 2.0 V and the I_{ON} well satisfies technology requirements, although I_{OFF} increases several orders of magnitude with increasing of V_{DS}. The threshold roll-offs effect was also weakened at V_{DS} = 2.0 V and V_{DS} = 3.0 V, as shown in Fig. 5f. If the MoS_2 FETs was bent, I_{ON} increases but the *SS* rapidly worsened. This can be explained that the pathway number in the integrated MoS_2 nanosheet networks increase at the bottom layer and the electrons mobility reduces after scattering, which results in I_{ON} enhancement but degraded *SS*.

For the double-gate junctionless device, the on-state current is increased. But for the single gate junctionless device, the coupling effect of vertical-field would disappear. Then the on-state current increases slightly with the increased channel thickness, even when the channel becomes very thick. Another key problem is the threshold voltage drift. When the thickness of the MoS_2 channel increases, and more electrons drift into the surface of channel, the threshold voltage drifts to the left (∼ 0.2 V) without exhausting electrons at the top MoS_2 layer.

In order to reduce the supply voltage and suppress the gate leakage current, recently, many new devices could be equipped to complement CMOS transistors. One of the most extensive research topics in this field is the tunnelling field-effect transistors (TFETs). The primary transport mechanism in a TFET is band-to-band tunneling (BTBT) which is different from the thermionic injection of electrons and can break through the limit of 60 mV/dec. Electrons and holes transfer from valence band into conduction band at a heavily doped p^+–n^+ junction, where the abruptly I_{ON}/I_{OFF} ratio can be controlled by channel band modulation. Although new structure device innovations have been proposed to reduce *SS* by scaling down [41, 42], quantum effects and short channel effects have limited voltage-scaling and device reliability issues.

The output and transfer curves of *n*-type MOS (NMOS) and TFET (*n*-TFET) can be simulated by commercial Silvaco ATLAS device simulator. These results were obtained by using a nonlocal BTBT model, bandgap-narrowing model, drift diffusion model and an abrupt doping profile, Shockley–Read–Hall (SRH) recombination model, Lombardi mobility model, optical phonon scattering (OP) and acoustic phonon scattering (AP) model, modified local-density approximation (MLDA) quantum effect model and Schenk trap-assisted tunnelling (TAT) model. For the *n*-TFET (p^+–*i*–n^+), the p^+ source doping concentrations is 1×10^{20} atom/cm^3, the channel is *p*-type intrinsic (*i*), and the n^+ drain is 1×10^{20} atom/cm^3. But for the NMOS (p^+–*i*–p^+), the only difference is the doping type of the source. The heavily *p*-type doping of source/drain is 1×10^{20} atom/cm^3, and the *n*-type intrinsic (*i*) channel is 1×10^{16} atom/cm^3. The channel width and length are 1 μm and 45 nm, respectively, and the SiO_2 gate oxide thickness is 10 nm. The electrical parameters of the Silicon-On-Insulator (SOI) *n*-TFET and NMOS have been optimized, which is as closely as possible to the 45 nm process node. Two main weaknesses of TFETs are the low on-state current and the ambipolarity because they depend on Wentzel–Kramer–Brillouinp (WKB) transmission probability and device symmetry, respectively.

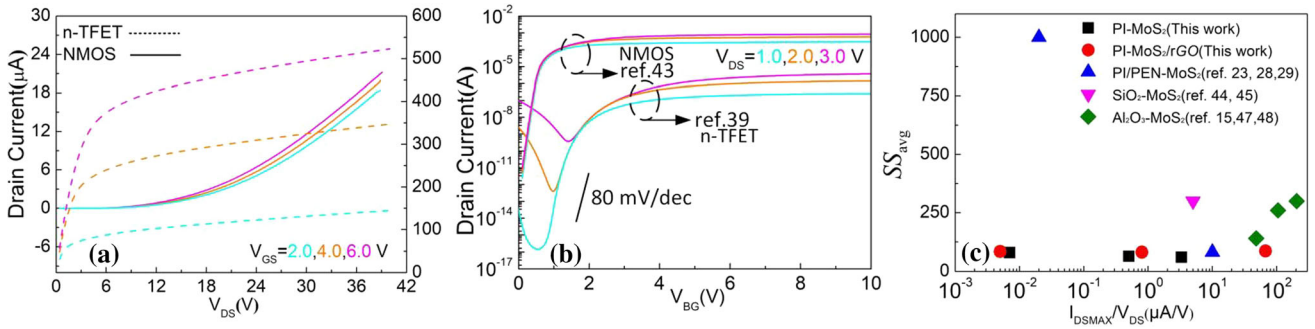

Figure 6 **a** The output characteristics of the NMOS and *n*-TFET, V_{DS} is in the range of 0–40 V, **b** transfer characteristics of the NMOS and *n*-TFET with width = 1 μm and channel length = 45 nm at different V_{DS}, and **c** a new method shows these performance of devices.

The output characteristics of the *n*-type MoS_2 FETs are similar to the *n*-TFET, as shown in Fig. 6a. One key point is that the output current of the NMOS is larger than that of low-power dissipation device due to the quantity of hot-carrier injection electrons from the source into channel. Unlike the NMOS, TFET leakage current increases for increasing V_{DS}. Traps can be captured by introducing trap states at the channel/oxide interface. The trap-assisted tunnelling process enhances more the leakage current and deteriorates *SS* of the *n*-TFET [43, 44] compared to the NMOS [45, 46], as shown in transfer curves in Fig. 6b. The experimental realization average *SS* of MoS_2 shows an advantage over the *n*-TFET and NMOS which strongly depend on the quality of novel 2D materials. Although the I_{ON}/I_{OFF} ratio and I_{OFF} (red circle in Fig. 6c) of PI substrate MoS_2 FETs are not optimal, the average *SS* of 75 mV/dec and 10^4 of I_{ON}/I_{OFF} characteristics are already close to actual industry requirements.

Besides, Fig. 6c shows the performance of devices made with our novel fabrication method. The better performance is near the right corner. Deji Akinwande's results illustrated the outstanding electron mobility properties of MoS_2 on a large-area flexible PI substrate with integrated high-κ dielectric [26]. Still, the *SS* on the polyethylene naphthalate (PEN) was not good as on PI. FETs were fabricated using MoS_2 inks on SiO_2 by a drop-casting process [47, 48], and the I_{ON}/I_{OFF} of 3×10^5 and *SS* are high values under a high-κ dielectric MoO [49]. MoS_2 nanoflakes are transferred on Al_2O_3-covered Si substrates [18, 50, 51], but the *SS* is also too high. Although FETs have undergone a process from simplicity to complexity, all-inkjet-printed MoS_2 technology on plastic substrates make 2D flexible device possible in this paper. Thus, as size scaling continues, all-inkjet-printed flexible MoS_2 FETs may be a better choice for flexible electronic applications.

Conclusions

In summary, flexible MoS_2 and MoS_2–rGO FETs were designed and manufactured through a simple all-inkjet-printed process. The results of our study show significant improvements in the drive current, I_{ON}/I_{OFF} ratio and *SS* to record levels in flexible printing technology. We also discussed the carrier transport characteristics of MoS_2 and MoS_2–rGO FETs under mechanical stress between two-dimensional material and the PI substrate. The biaxial tension introduced by mechanical stress is the condition that mainly influences the electrical characteristics of the all-inkjet-printed FETs. Despite of electrical performance degradation of FETs caused by bending; nevertheless, the I_{ON} of MoS_2 FETs was improved. Consequently, the flexible PI substrate MoS_2 FETs and the print processing method we demonstrated here have great application potential due to its large area and bulk production. Moreover, in comparison with conventional fabrication techniques, our printing processing is straightforward for thin film transistors development and fabrications.

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Compliance with ethical standards

Conflict of interest All authors declare that they have no conflict of interest.

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