Applied Nanoscience
https://doi.org/10.1007/s13204-020-01438-3

ORIGINAL ARTICLE

All-inkjet-printed MoS_2 field-effect transistors on paper for low-cost and flexible electronics

Zhi Jiang[1,2] · Long Chen[1] · Jin- Ju Chen[1] · Yan Wang[1] · Zhao- quan Xu[1] · Enrico Sowade[3] · Reinhard R. Baumann[4] · Evgeniya Sheremet[5] · Raul D. Rodriguez[5] · Zhe- sheng Feng[1]

Received: 2 April 2020 / Accepted: 27 April 2020

Abstract

All-inkjet-printing of transistors has received much attention for low cost and flexible integrated circuits. However, most flexible field-effect transistors (FETs) based on the emerging two-dimensional materials suffer from the high cost of substrate and electrode materials. The requirements for high-temperature synthesis and precise control in processing add another layer of complexity. To overcome these issues, low-cost flexible paper-based MoS_2 FETs were fabricated by inkjet printing of MoS_2 channel materials on paper. Additionally, we proposed and achieved the mask-less and low-temperature formation of source and drain electrodes on paper using in-situ selective-area copper reduction. A low sub-threshold swing of 80 mV/dec, high on/off ratio of 10^5, and very high turn-on current (I_{on}) of 200 µA of the paper-based flexible MoS_2 FETs were demonstrated using the proposed low-cost and facile all-inkjet-printing technique. The all-inkjet-printing technique assisted by in-situ copper reduction opens new opportunities for low-cost and batch fabrication of paper-based electronic devices in ambient conditions.

Keywords MoS_2 · Sub-threshold swing · FETs · Nanosheets

Introduction

MoS_2 is one of the emerging materials for flexible electronics because of its unique tunable bandgap (direct bandgap $E_g = 1.8$ eV for monolayer and indirect bandgap $E_g = 1.2$ eV for multilayer) and mechanical stability (Chung et al. 2014; Yao et al. 2013; Kim et al. 2016). Flexible MoS_2 field-effect transistors (FETs), photoelectric sensors, and logical switches were reported, showing its potential applications in wearable electronics (Alsaif et al. 2016; Kim et al. 2012; Lim et al. 2018; Das et al. 2013; Li et al. 2015a; Ziyu et al. 2018, 2019, 2020). Although few-layer MoS_2 was reported to exhibit a high current on/off ratio of 1×10^8 and an electron mobility of 200 $cm^2/(V\ s)$, the bottom-up approaches of chemical vapor deposition (CVD) or atomic layer deposition (ALD) of MoS_2 thin films often require transferring to high-κ dielectrics, and hence suffer from relatively low yield (Shin et al. 2018; Lee et al. 2015; Miyoshi et al. 2015). To improve the scalability and reduce cost, top-down methods, such as inkjet printing technology, were reported for the fabrication of FETs based on layered MoS_2 nanosheets (Castro et al. 2015; Li et al. 2016; Liu et al. 2015). MoS_2 inks

Electronic supplementary material The online version of this article (https://doi.org/10.1007/s13204-020-01438-3) contains supplementary material, which is available to authorized users.

✉ Jin- Ju Chen
jinjuchen@uestc.edu.cn

✉ Enrico Sowade
enricoso@gmx.de

✉ Zhe- sheng Feng
fzs@uestc.edu.cn

[1] School of Materials and Energy, University of Electronic Science and Technology of China, Chengdu 610054, China

[2] Institute of Fundamental and Frontier Sciences, University of Electronic Science and Technology of China, Chengdu 610054, China

[3] R&D Digital Printing, Zschimmer & Schwarz Mohsdorf Gmbh & Co.kg Ltd, 09217 Burgstädt, Germany

[4] Digital Printing and Imaging Technology, Technische Universität Chemnitz, 09126 Chemnitz, Germany

[5] Tomsk Polytechnic University, 30 Lenin Ave, Tomsk, Russia

Published online: 16 May 2020

are obtained using liquid-phase sonication-assisted exfoliation. Few-layer, bilayer, and even monolayer MoS_2 nanosheets can be obtained. With intense research efforts on semiconductor inkjet printing, large-scale and low-cost all inkjet-printed flexible FETs have become a reliable and direct writing technology. Such dispersed nanosheets can form a device channel by continuous inkjet printing technology. Nanomaterials are widely used to develop novel environment friendly chemical mechanical polishing slurries (Zhenyu et al. 2012a, 2012b, 2013, 2018, 2020; Jing et al. 2019). However, interconnected networks based on gate-patterned FETs are still difficult to obtain with full self-alignment insulator-covered gate technology, nanoscale precision wafers and substrates are fabricated for the use in high performance devices of semiconductor and microelectronics industries. Such random MoS_2 nanosheets network channel has very limited mechanical resilience, breaking after hundreds of bending cycles (Bo et al. 2018; Zhenyu et al. 2015; Zhang et al. 2015). Therefore, reported flexible devices usually have low on-state current and poor sub-threshold swing (SS) when produced at large-scale, compared with traditional rigid ones (Shokouh et al. 2015; He et al. 2012; Zhenyu et al. 2017). Another challenge in the fabrication of flexible FETs is that the electrodes must be reliable in bending or folding tests. The mechanical adhesion between a metal electrode, e.g. silver, and a substrate, e.g. polyimide film, is poor (Li et al. 2014, 2015b; Castro et al. 2014; Akinwande et al. 2014). Additionally, silver electrodes were printed by expensive the Dimatix Materials Printer (DMP) 2000/3000 series inkjet printers, are not cost-effective. These studies are a breakthrough and milestone contribution compared with conventional industries, eliminating the pollution dramatically to the environment (Zhang et al. 2020; Cui et al. 2019; Junfeng et al. 2019).

In this paper, we propose and demonstrate a process that allows the effective and large scale production of all-inkjet-printed MoS_2 FETs on mechanically flexible paper substrates. Few-layer MoS_2 nanosheets, acting as the active channel of a FET, were printed with a conventional desktop printer (EPSON-LP310) on a pre-formed electrode array. The electrode array was made by in situ reduction of copper (Cu), i.e. selective area reduction at inkjet-printed areas. This method not only provides excellent mechanical adhesion of electrodes but also offers an effective means for low-cost fabrication of flexible electronics. Despite the paper surface roughness, the printed MoS_2 nanosheets can be firmly attached to the paper surface, which is beneficial for flex resistance. More importantly, a remarkable SS ranging from 80 to 90 mV/dec was demonstrated experimentally in back-gated FETs. The MoS_2 FETs show a high on/off ratio of 10^5, a small threshold voltage roll-off range from − 1 to 1 V, and a high on-state current (I_{on}) at a low drive voltage V_{ds} of 3.0 V.

Results and discussion

We designed and implemented a process for the large-scale production of MoS_2 FETs using paper as the substrate and the gate dielectric. Figure 1a, b shows the sequential fabrication process of source/drain gate electrodes and channel layers of the all inkjet-printed MoS_2 FETs on paper. Initially, $AgNO_3$ precursor ink was deposited on the back of a piece of paper, and then printed into strip patterns by inkjet printing. An optical image of $AgNO_3$ precursor strips printed on paper is shown in Fig. 1c. After UV curing of the $AgNO_3$ precursor ink, in-situ Cu reduction was simultaneously conducted at the strip patterns and the back of the paper. The paper with cured $AgNO_3$ patterns was immersed in a Cu-containing catalyst solution. The source and drain electrodes were selectively formed at the pre-printed $AgNO_3$ strips by Cu reduction reaction in a Cu-containing catalyst solution at a low temperature of 60 °C, as illustrated in Fig. 1a. Figure 1d shows the Cu source/drain electrodes and the back-gate electrode deposited on the pristine paper. The Cu source/drain electrodes adopted exactly the shape of the $AgNO_3$ precursor strips through the in-situ selectively area Cu reduction reaction. The MoS_2 ink (Fig. 1b and S1) was printed directly on Cu electrode arrays on the paper surface to form MoS_2 channel and thus one can greatly reduce the complexity in the flexible device fabrication. The MoS_2 ink was dried at 40 °C to remove ethanol and deionized water in polyvinyl pyrrolidone (PVP), and MoS_2 channels with a length of 100 µm and widths of 100 µm and 1000 µm were formed. After the low- temperature annealing step, the all-ink-printed MoS_2 FETs were fabricated on paper, Fig. 1e shows the optical images of the fabricated transistors. Figure 1f shows the three-dimensional schematic of the paper-based MoS_2 FET. The effective channel length is controlled by the distance between the deposited Cu source and drain contacts.

Figure 2 shows the top-view and cross-sectional scanning electron microscopy (SEM) images of the MoS_2 transistors printed on paper. As shown in Fig. 2a, well-defined Cu electrodes are observed. The chemical composition of the deposited Cu electrodes was analyzed by energy-dispersive X-ray spectroscopy (EDS), as shown in Figure S2a, b. The back-gated MoS_2 FET printed on Cu electrode arrays was show confirmed by the EDS results. The Cu film also contains nickel and iron residues that originate from the Cu-containing catalyst solution. The gap between the two electrodes is smaller than the initial template made by $AgNO_3$ strip patterns (100 µm). The reduced channel width is due to the invasion effect of $AgNO_3$ and swelling during Cu-reduction. The Cu films are compact with

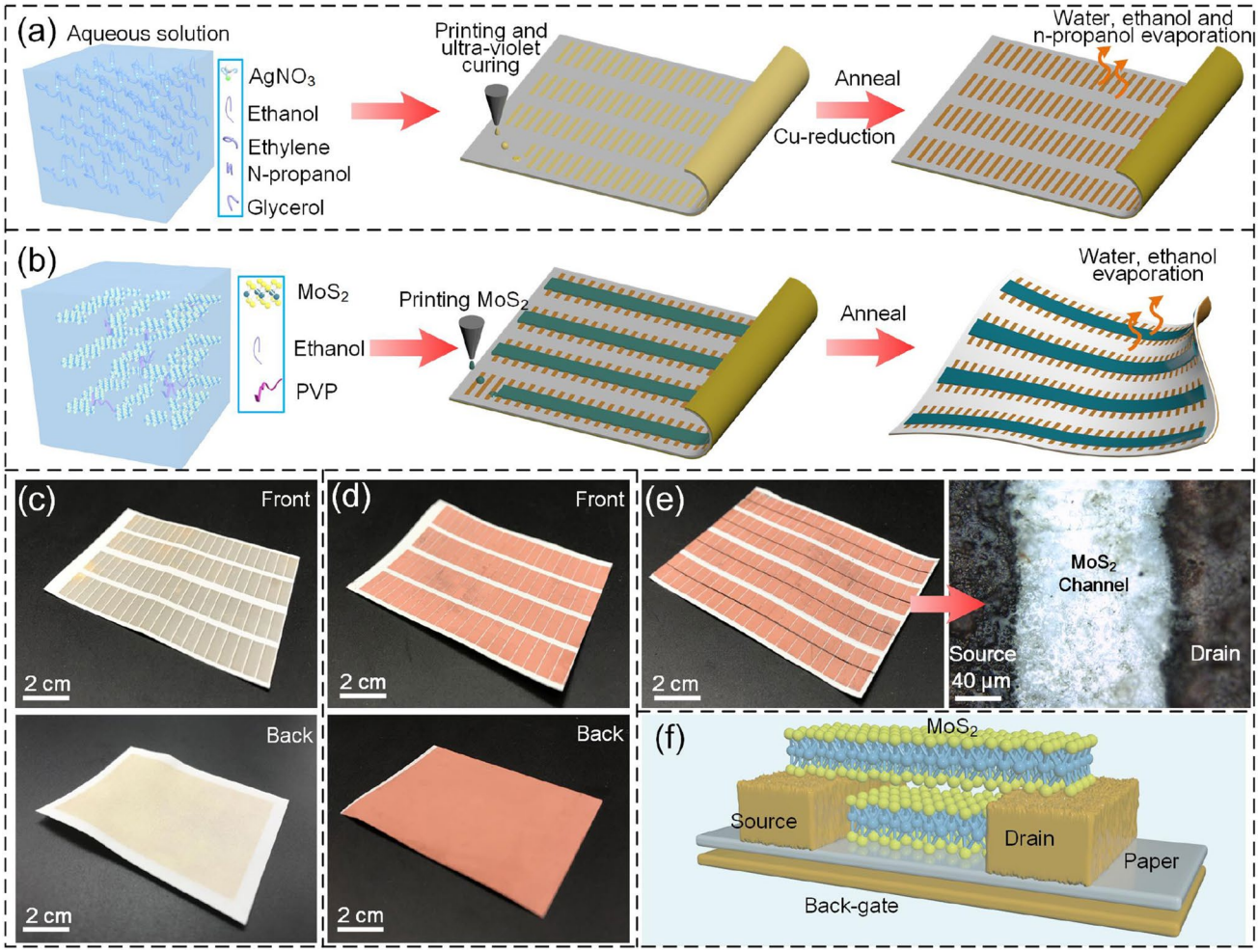

Fig. 1 The detailed fabrication process of the paper-based MoS_2 FETs. **a** $AgNO_3$ ink was prepared and printed on paper, the pristine $AgNO_3$ electrode patterns were obtained after ultra-violet curing, Cu electrodes arrays were then selectively reduced from the $AgNO_3$ patterns with HCHO catalyst at 60 °C. **b** Liquid-phase exfoliation to form few-layer MoS_2 nanosheet ink stabilized with PVP. The MoS_2 channel was printed between the Cu source/drain electrodes on paper, and then the MoS_2 channels was annealed at a temperature over 40 °C to remove deionized water and ethanol. **c** Optical images of printed $AgNO_3$ seed patterns on both sides of the paper. **d** Optical images of Cu electrodes formed after selective reduction. **e** An optical image shows the fabricated MoS_2 FET array printed on paper, and a magnified MoS_2 FETs. **f** Schematic illustration of a MoS_2 FET on paper substrate

small bumps, as shown in the SEM image of Fig. 2a. The film roughness be related to Cu can be explained by the formation of Cu clusters of different sizes as indicated in the inset of Fig. 2a. Most of these bulges could reduction at 60 °C. Figure 2b shows the SEM image of MoS_2 ink printed on the Cu electrodes. A compact MoS_2 film is formed over the electrodes with sharp interface, which show the potential to achieve narrow channel width. To investigate the quality of MoS_2 films deposited by inkjet printing, X-ray diffraction (XRD) measurements are conducted. The diffraction patterns dominated by the bulk MoS_2 (002) peak for films obtained at different exfoliation times, indicating that few-layer or bilayer MoS_2 nanosheets are restacked after drying. There are three diffraction peaks centered at 14.4°, 44.1°, and 60.1°, which are indexed as (002), (006) and (008), respectively, as shown in Fig. S2b. It is confirmed that the stacked nanosheets of the two-hexagonal (2H) phase are randomly arranged during ultrasonic liquid-phase exfoliation. With ultrasonic exfoliation time increasing, the (100) peak at $2\theta = 34.3°$ becomes increasingly apparent, and this observation shows that the PVP/MoS_2 ink consists of 2D MoS_2 nanosheets.

Figure 2c shows the cross-section morphology of the MoS_2 film. The low-magnification SEM image shows that the thickness of the MoS_2 film is rather uniform across a large area. The thickness of the printed MoS_2 channel is *ca.* 5 μm as shown in Fig. 2d. Beneath the MoS_2 film, the Cu atoms are agglomerated as displayed in Fig. 2c, which may improve electron injection from the Fermi level of Cu contacts to the electron injection from the Fermi level

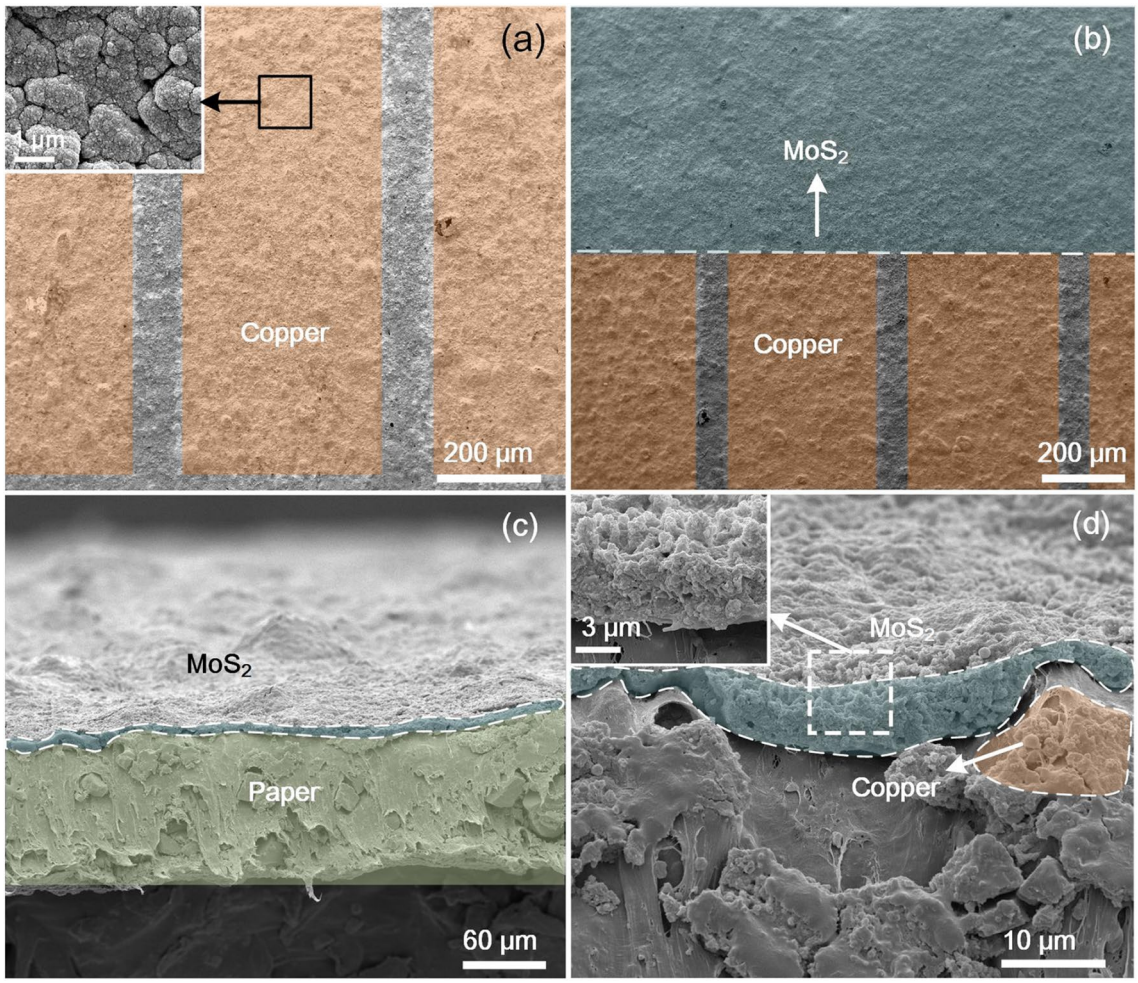

Fig. 2 SEM images of **a** the front of source/drain electrodes without printing MoS_2 active channel and **b** a 100 µm MoS_2 channel length was printed on the paper, **c** SEM pictures of the surface of MoS_2 channel and **d** the contact between copper and MoS_2 channel

of Cu contacts to the conduction band of the conduction band of the MoS_2 channel.

Since the Cu source and drain electrodes are placed further apart (100 µm), it is necessary to evaluate MoS_2 nanosheets' size and ensure the interconnection between nanosheets in the device channel. The few-layer thickness of nanosheets is confirmed by transmission electron microscopy (TEM) images shown in Fig. 3. To demonstrate the sonication time effect on exfoliation, the pristine MoS_2 was sonicated for different times: 3 h, 24 h, and 48 h with PVP. Due to electrostatic repulsion, the surface energy of PVP, and van der Waals (vdWs) forces in MoS_2, these nanosheets are stable in the chemical solution. High-resolution TEM (HRTEM) was also employed to investigate the structural properties of MoS_2 nanosheets. Although the TEM measurements did not provide the layer number of MoS_2 nanosheets, the thickness of MoS_2 crystal can be indicated by its transparency.

Figure 3a shows a pristine MoS_2 crystal containing a large quantity of small MoS_2 nanosheets. The typical size of the MoS_2 crystal is about 4 µm. A MoS_2 transistor based on the pristine MoS_2 crystal is rather poor in our tests, in terms of SS and on/off current ratio. After 3-h sonication, the size of a MoS_2 crystal is about 500 nm as shown in Fig. 3b. HRTEM image in Fig. 3c shows a number of small size multilayer MoS_2 nanosheets covering the MoS_2 crystal due to insufficient ultrasonic exfoliation. Although there are still some un-exfoliated MoS_2 crystals, the layered MoS_2 crystals have become increasingly thin.

After 24 h' exfoliation, as shown in Fig. 3d, the MoS_2 nanosheet thickness and size (*ca.* 300 nm) was further reduced. Figure 3e shows a magnified TEM image of a MoS_2 nanosheet. Multiple stacked MoS_2 layers are clearly observed. The inset of Fig. 3e shows the Fast Fourier transform (FFT) of the multilayer MoS_2, which shows a good single crystal structure. Compared with the MoS_2 sheets

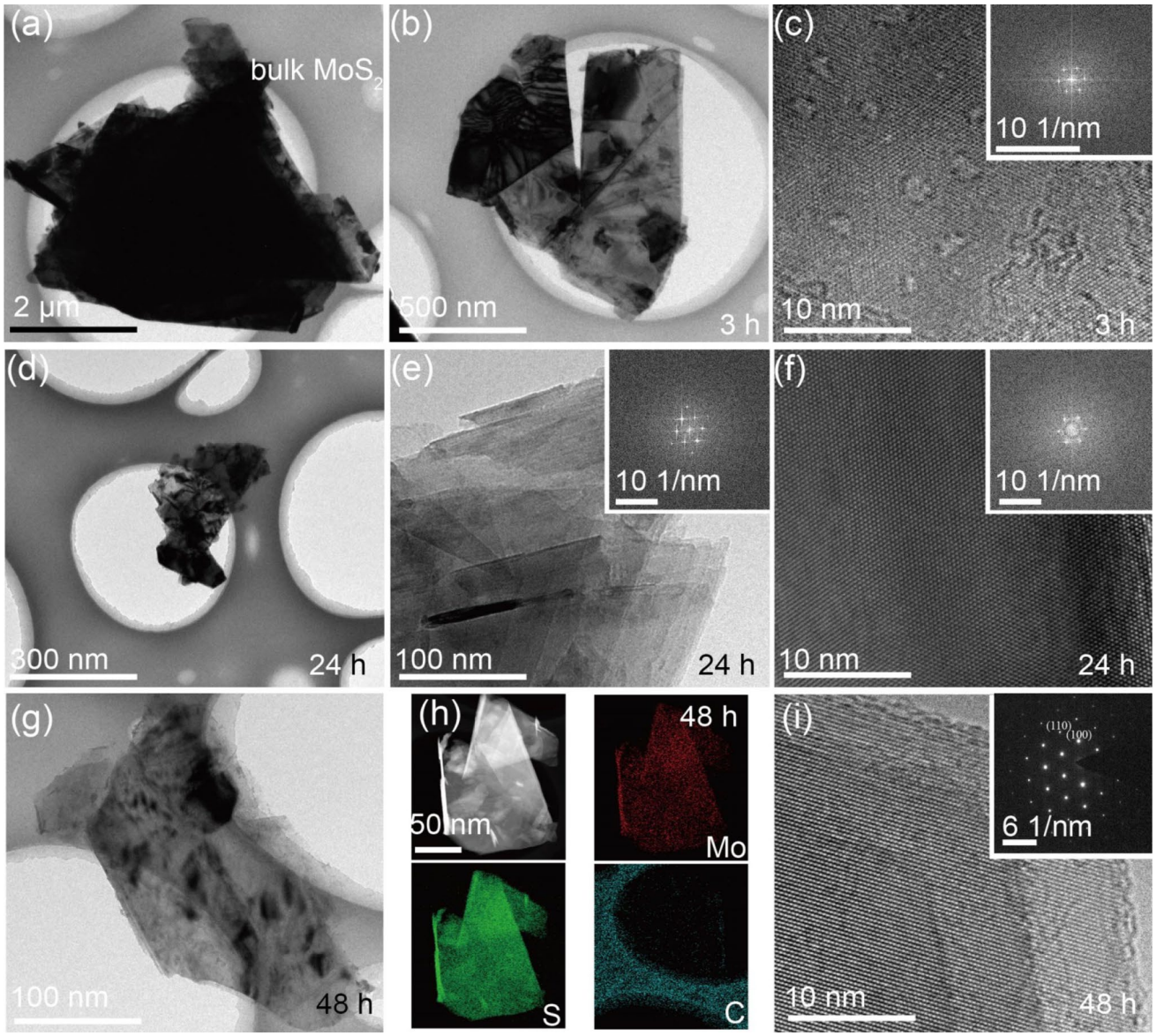

Fig. 3 TEM images of **a** the pristine bulk MoS_2 and **b** the exfoliated MoS_2/PVP crystals dispersed in ethanol after 3 h sonication at 70 W. **c** HRTEM image of MoS_2 nanosheets showing protuberant texture due to the overlap of small size MoS_2. **d** TEM image of MoS_2 crystals after exfoliation with ultrasound for 24 h. **e** The stack structure of MoS_2 nanosheets after 24 h sonication exfoliation and its corresponding Fast Fourier transform (FFT) shown in the inset. **f** HRTEM image of few-layer MoS_2 nanosheets without multiple small-sized MoS_2 layers after 24 h' sonication exfoliation and the corresponding FFT pattern. **g** TEM image of few-layer MoS_2 nanosheet after 48 h sonication exfoliation. **h** TEM-EDS images of few-layer MoS_2 (48 h) and elemental mapping results on carbon framework. **i** HRTEM image of the selected region of few-layer MoS_2 nanosheets and its corresponding six-fold-symmetric diffraction spots SAED pattern

(3 h sonication) shown in Fig. 3c, small MoS_2 nanosheets stacked on a large size crystal do not appear, as shown in the HRTEM image of Fig. 3f. Defect-free lattice fringes of the MoS_2 nanosheets and FFT are clearly shown in Fig. 3f and the inset, respectively.

After 48-h sonication, a stable MoS_2 ink solution was obtained (Fig. S1). The TEM image in Fig. 3g illustrates the lateral sizes and the layered structure of nanosheets obtained after 48 h of ultrasonic exfoliation. The lateral size was mainly distributed between 100 and 200 nm. The TEM-EDS elements mapping analysis of the MoS_2 nanosheets are presented in Fig. 3h. Elemental C originates from the ultrathin carbon-copper film substrate used for TEM analysis. Mo/S atomic ratio of few-layer MoS_2 nanosheets is about 1/2, which indicates ultrasonic exfoliation did not induce an unacceptably high defect concentration. This is a key observation since otherwise a highly defective MoS_2 channel increases the carrier scattering, compromising the

device performance. HRTEM image in Fig. 3i confirms the formation of a dispersive layer structure made of MoS_2 nanosheets. As the number of layers decreases, trilayer, and even bilayer MoS_2 nanosheets are possible. Few-layer MoS_2 crystals are critical for the formation of a continuous MoS_2 channel. The corresponding selected area electron diffraction (SAED) pattern is shown in the inset of Fig. 3i, confirming the hexagonal structure of MoS_2 and the diffraction spots for the (110) and (100) planes along the < 100 > crystal axis.

The electrical characterizations, the *I*–*V* transfer and output characteristics of the MoS_2 FETs, were performed using a semiconductor analyzer (Agilent B1500a). The paper-based MoS_2 FET exhibits a typical *n*-type behavior, where the thickness of the oxide is kept constant at 100 µm. The experimental and simulated Non-Equilibrium Green Functions (NEGF) results (Fig. 3s) are obtained varying the source-to-drain bias (V_{ds}) from − 2 to 2 V and back-gated (V_{gs}) from 1 to 40 V in steps of 1.0 V, as shown in Fig. 4a. By taking optical phonon and acoustic phonon scattering into consideration, the simulated NEGF output currents agree with experimental values well. Therefore, the layered MoS_2 FET carrier transport probably presents multilayer optical phonon and acoustic phonon scattering. To evaluate the flexibility of our paper-based MoS_2 FETs, the MoS_2 FET array is bent at different angles under mechanical stress, as shown in Fig. 4b, c. A typical Ohmic contact behavior in the I_{ds}–V_{ds} output characteristics is observed at various V_{bg} after bending at 170° and 130°. Here, the output currents are the smallest for the largest bending angle and gradually decreased when increasing the bending angle. These results can be explained due to an increase of their respective contact resistance between the channel and source, so

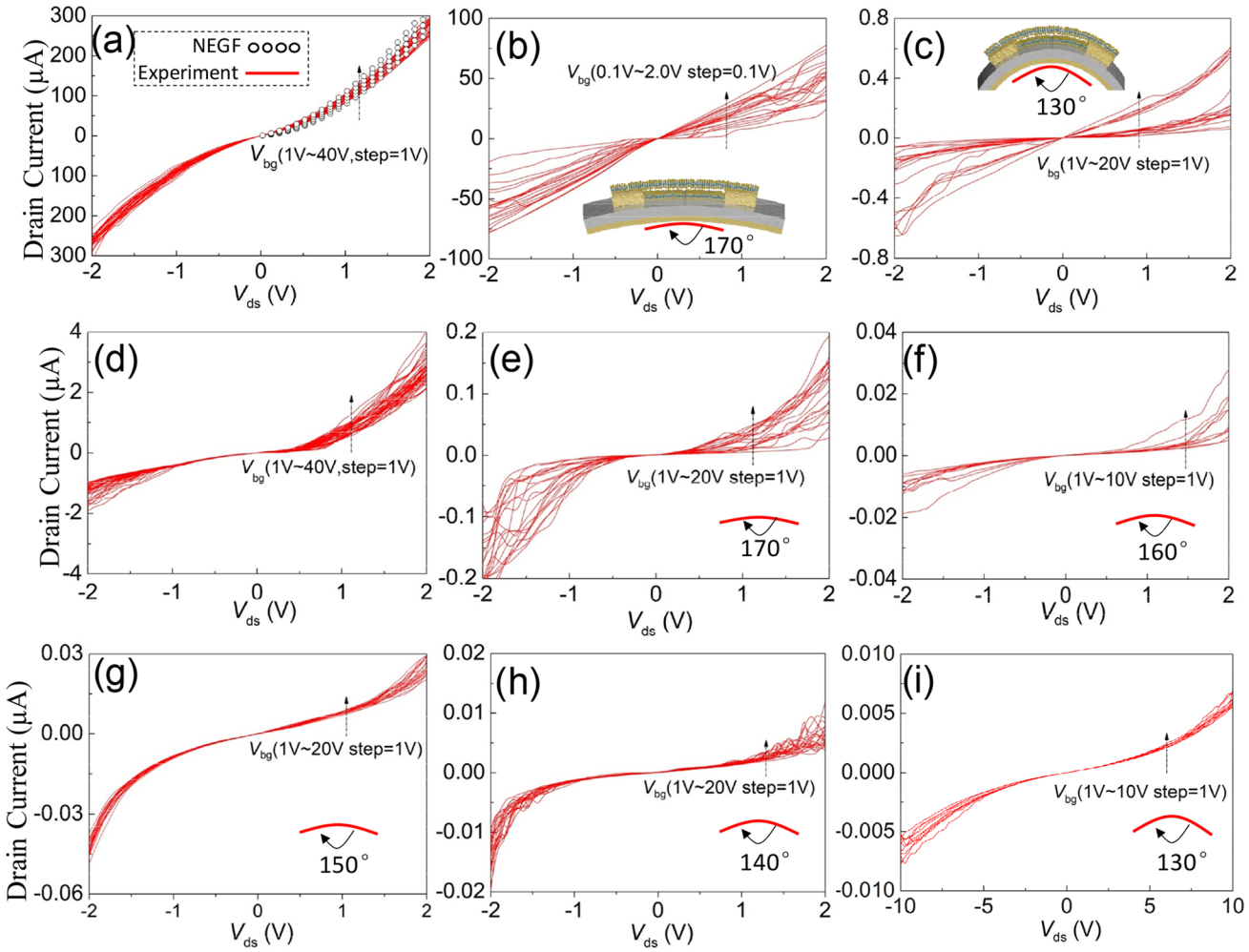

Fig. 4 Electrical properties of flexible Cu/MoS_2 contact FET under initial flat and bent condition. Output characteristics drain-to-source current versus drain-to-source voltage (I_{ds}–V_{ds}) curves under different gate bias V_{gs} show typical *n*-type gate dependence. MoS_2 FET with channel width (W_g = 1000 µm) and length (L_g = 100 µm) at various bend angles, **a** the NEGF simulation results were compared with experimental results w/o bending (V_{bg} is in the range of 1–40 V), **b** bending angle is 170°, **c** 130°. MoS_2 FET with channel width (W_g = 100 µm) and length (L_g = 100 µm) at various bending angles **d** flat, **e** 170°, **f** 160°, **g** 150°, **h** 140°, and **i** 130°

carrier transmission coefficient decreases (Guo et al. 2014; Bartolomeo et al. 2018).

Figure 4d–i shows the output characteristic curves of the MoS_2 FETs with a narrow channel width, $W_g = 100$ µm, at different bending angles. Although the channel width reduced from 1000 to 100 µm, the output currents scaled down more than ten times due to the non-uniform distribution of MoS_2 nanosheets, and hence random interconnection networks in the channel. For the channel width of 100 µm, the *I–V* characteristics of MoS_2 FETs bending at 170°, 160°, 150°, 140°, and 130° are shown in Fig. 4e–i, respectively. The output current generally decreased with increasing bending angle. This current reduction is attributed to a random interconnecting network with reduced overlapping, and every transistor remains a constant degree after hundreds of bending. Table 1 shows the maximum on-state current at different bending angles, and the on-state current would become weaken as the effective interconnection networks decrease.

To further elucidate the MoS_2 FETs stability, the transfer curves from day 1 up to 30 days were analyzed. These results are presented in Fig. 5a for a MoS_2 FET with $W_g = 1000$ µm and $L_g = 100$ µm showing an obvious negative threshold voltage (V_{th}) shift as the transistor ages. Threshold voltages are usually defined by the I_{ds}–V_{bg} characteristics by an abrupt current increase behavior in the sub-threshold region. It is worth noticing that the V_{th} shifted as the FETs aged, but the I_{on}/I_{off} ratio is preserved to ~ 10^4 and the SS ~ 80 mV/dec. The different I_{off} between Fig. 5a, b may originate from different interconnection network paths at the same drive voltage V_{ds}. Additionally, the simulation NEGF results show different *SS* in the linear range. Since the NEGF calculated an integrated 2D MoS_2 channel, but the experimental interconnection networks most likely contain several parallel

Table 1 Different device width of experimental results at various bending angles

Bending angle	I_{MAX}, Flat (0°) at $V_{ds} = 2$ V	I_{MAX}, 170° at $V_{ds} = 2$ V	I_{MAX}, 160°at $V_{ds} = 2$ V	I_{MAX}, 150° at $V_{ds} = 2$ V	I_{MAX}, 140° at $V_{ds} = 2$ V	I_{MAX}, 130° at $V_{ds} = 2$ V
Device size						
$W_g = 1000$ µm, $L_g = 100$ µm	210 µA	68 µA	x	x	x	0.63 µA
$W_g = 100$ µm, $L_g = 100$ µm	2.5 µA	57 nA	43 nA	28 nA	17 nA	5 nA

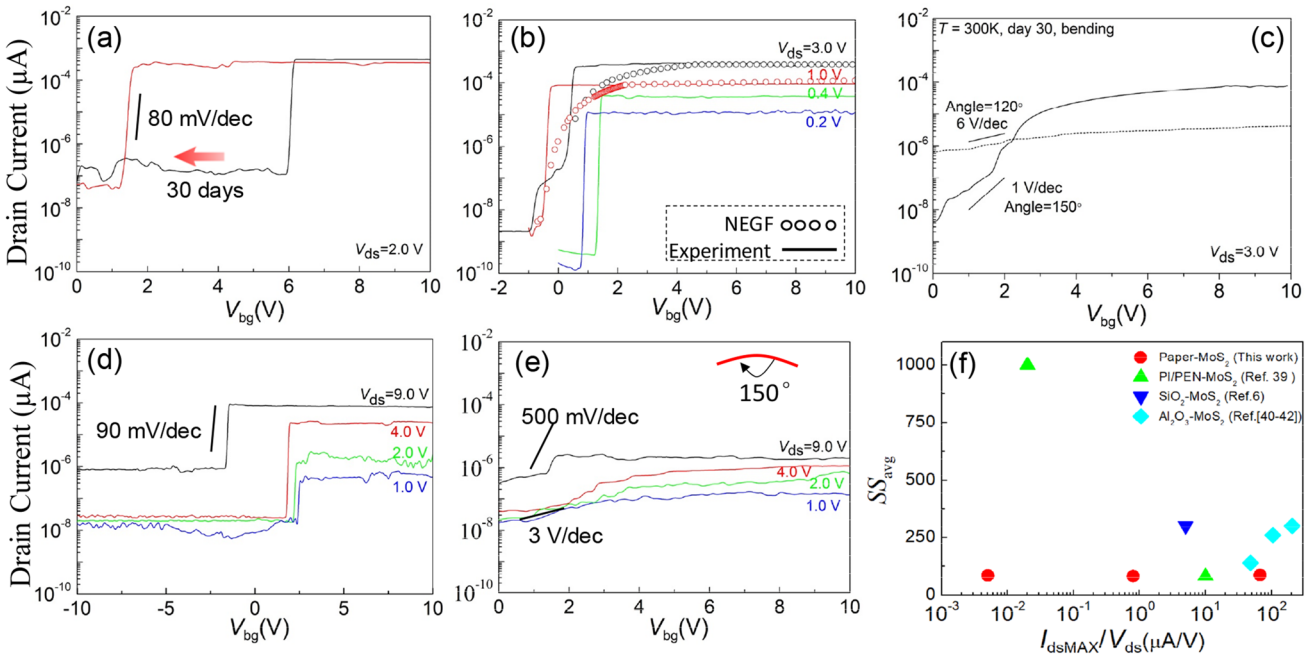

Fig. 5 The transfer characteristics of MoS_2 FET with $W_g = 1000$ µm and $L_g = 100$ µm of drain-to-sourcecurrent versus back-gated voltage (I_{ds}–V_{bg}) curves **a** at V_{ds} = 2.0 V versus age after day 30 in air, showing a negative V_{th} shift, **b** NEGF and experimental results were investigated at different V_{ds} without bent after day 30 and **c** the transfer characteristics under different bending angles (120° and 150°); The transfer characteristics of MoS_2 FET with W_g = 100 µm and L_g = 100 µm under different bending angle **d** flat, and **e** 150° at different V_{ds} after day 30. **f** A new method shows these performances of MoS_2-based on different substrates

paths. Hence, with an increase in V_{bg}, one of the interconnection network paths could firstly reach current saturation with small V_{ds}. The variation of the V_{th} values is estimated to be shifted (from 1.2 to − 1.0 V) due to the random network path. As V_{ds} increases further, the interconnection networks will be significantly increased, which can be confirmed by the rapid increase of the saturation current at high V_{ds} (3.0 V). Figure 5c shows a comparison of the transfer characteristics of MoS_2 FET ($W_g = 1000$ µm and $L_g = 100$ µm) under different bending angle 120° and 150°. As the bending angle increases, the SS is far worse than the value of 80 mV/dec obtained without bending.

The transfer characteristics of MoS_2 FET ($W_g = 100$ µm and $L_g = 100$ µm) showed I_{on}/I_{off} ratio only ~ 10^2 and SS of 90 mV/dec at $V_{ds} = 9.0$ V, as shown in Fig. 5d. The reduced on-state current could be attributed to a reduction of interconnection networks path. The threshold voltage for $V_{ds} = 1.0$ V, 2.0 V, 4.0 V and 9.0 V were found to be 2.4 V, 2.2 V, 1.9 V, − 2.0 V, respectively. After bending 150°, the SS becomes worse from 500 mV/dec to 3 V/dec at $V_{ds} = 9.0$ V and 1.0 V respectively, as shown in Fig. 5e. As the V_{ds} increases further, the Schottky barrier height and carrier electron injection efficiency is reduced and improved, respectively, for larger bias voltage across the Cu-MoS_2 contact junction. Figure 5f shows the performance of devices made with the paper-based MoS_2 FETs. If symbol is near the right corner, the performance shall show good according to our new representation method. The outstanding electron mobility properties of MoS_2 on a large-area flexible PI substrate were illustrated (Akinwande et al. 2018). FETs were hand-made by ink-jetting MoS_2 inks on SiO_2 by a drop-casting process (Lim et al. 2018). MoS_2 nanoflakes are transferred on Al_2O_3-covered Si substrates (Shih et al. 2014; Hui et al. 2016; Jiahao et al. 2014), but the SS is also too high. Although FETs have undergone a process from simplicity to complexity, the all-inkjet-printed technology on paper substrates make MoS_2 flexible devices possible.

Conclusion

In summary, the flexible paper substrate n-type MoS_2 FETs on paper were fabricated and manufactured through the all-inkjet-printed process. The MoS_2-based device on paper exhibits an on/off current ratio of 10^5 and also achieve good SS of 80 mV/dec with $W_g = 1000$ µm and $L_g = 100$ µm at $V_{ds} = 1.0$ V, which is an important factor for application in high-speed circuits. We also discussed the carrier NEGF transport characteristics by matching to experimental results in a flat state. The transfer characteristics curves obtained at different bending angles show an influence of mechanical deformation in the electrical characteristics of the all-inkjet-printed FETs. However, MoS_2 FETs show current characteristics and performance self-recovery after the mechanical deformation is released and the device is back to a flat state. Consequently, the flexible paper substrate MoS_2 FETs have great applications in logic circuits, mainly due to their large-area, bulk-production, and low-cost print process in contrast to conventional fabrication techniques for thin-film transistors.

Experimental section

Preparation of MoS_2 ink

MoS_2 powders are exfoliated in lift-assisted PVP and ethyl alcohol through bath sonication and centrifugation (7500 rpm) to obtain small MoS_2 nanosheets. Ethanol (20 ml) and deionized water (20 ml) were put in a sealed container mixed with PVP (80 mg), MoS_2 (440 mg), and sonicated at 27 °C for 48 h. The resultant suspension was centrifuged at 7500 rpm for 15 min to sediment thick nanosheets and the supernatant was obtained. Then, a stable MoS_2/PVP (2.4 mg/ml after evaporation of ethanol) dispersion was obtained.

Inkjet printing and electrode patterns

A redesigned commercial printer Epson-L310 was used to print the MoS_2 and $AgNO_3$. $AgNO_3$ ink was prepared with inorganic solvents, ethanol/water/ethylene glycol/n-propanol/glycerol. $AgNO_3$ electrodes pattern could be obtained via ultra-violet curing technique, the main concerns are the curing speed, and then Cu-containing catalyst solution consisted of $CuSO_4{\cdot}5H_2O$, $NiSO_4$, $K_4Fe(CN)_6$, $C_4H_4KNaO_6{\cdot}4H_2O$, $C_{10}H_8N_2$, and HCHO at an appropriate ratio that were injected to deionized water (10 g/L, 3 g/L, 0.04 g/L, 30 g/L, 0.02 g/L, 20 ml/L) in sequence, and the reaction of reduced Cu crystal particle is supposed to be the electrodes on surface of paper from Cu-containing catalyst solution with HCHO. MoS_2 channel layer was printed between the source/drain electrodes on paper by EPSON-L310. The deionized water and ethanol in the MoS_2 channel evaporate away over 40 °C for 10 min.

Characterization

Morphology of samples was observed by SEM (FEI NanoSEM50) Chemical identification of MoS_2 nanosheets was conducted by XRD (MAXima XRD-7000). Micro-level structure was characterized by TEM (FEI Tecnai G2F20 S-Twin). The direct current characteristics *I–V* curves of MoS_2 FETs were carried out using an Agilent parameter analyzer B1500a.

Acknowledgement This work was financially supported by Sichuan Science Technology Program (Grant 2018HH0152 and 2019YJ0196) and National Natural Science Foundation of China (Grant 51902040). ES and RDR acknowledge Tomsk Polytechnic University Competitiveness Enhancement Program 5-100.

Compliance with ethical standards

Conflict of interest There are no conflicts to declare.

References

Akinwande D, Petrone N, Hone J (2014) Two-dimensional flexible nanoelectronics. Nat Commun 5:1–12

Akinwande D, Petrone N, Hone J (2018) Two-dimensional flexible nanoelectronics. Nat Commun 5:5678

Alsaif MMYA, Chrimes AF, Daeneke T et al (2016) High-performance field effect transistors using electronic inks of 2D molybdenum oxide nanoflakes. Adv Func Mater 26:91–100

Bo W, Zhang ZY, Chang KK et al (2018) New deformation-induced nanostructure in silicon. Nano Lett 18:4611–4617

Castro HF, Sowade E, Rocha JG et al (2014) All-inkjet-printed bottom-gate thin-film transistors using UV curable dielectric for well-defined source-drain electrodes. J Electron Mater 43:2631–2636

Castro HF, Sowade E, Rocha JG et al (2015) Degradation of all-inkjet-printed organic thin-film transistors with TIPS-pentacene under processes applied in textile manufacturing. Org Electron 22:12–19

Chung JW, Ko YH, Hong YK et al (2014) Flexible nano-hybrid inverter based on inkjet-printed organic and 2D multilayer MoS2 thin film transistor. Org Electron 15:3038–3042

Cui J, Zhang Z, Liu D et al (2019) Unprecedented piezoresistance coefficient in strained silicon carbide. Nano Lett 19:6569–6576

Das S, Chen HY, Penumatcha AV et al (2013) High performance multilayer MoS2 transistors with scandium contacts. Nano Lett 13:100–105

Di Bartolomeo A, Grillo A, Urban F et al (2018) Asymmetric Schottky contacts in bilayer MoS_2 field effect transistors. Adv Func Mater 28:1800657

Guo Y, Han Y, Li J et al (2014) Study on the resistance distribution at the contact between molybdenum disulfide and metals. ACS Nano 8:7771–7779

He Q, Zeng Z, Yin Z et al (2012) Fabrication of flexible MoS_2 thin-film transistor arrays for practical gas-sensing applications. Small 8:2994–2999

Hui Y, Guangjun C, Sheng Y et al (2016) Field effects of current crowding in metal-MoS_2 contacts. Appl Phys Lett 108:103505

Jiahao K, We L, Kaustav B (2014) High-performance MoS_2 transistors with low-resistance molybdenum contacts. Appl Phys Lett 104:093106

Jing Z, Dongpeng M, Andrew TSW et al (2019) Micro/nano-structured ultrathin g-C_3N_4/Agnanoparticle hybrids as efficient electrochemical biosensors for L-tyrosine. Appl Surf Sci 467:608–618

Junfeng C, Zhenyu Z, Haiyue J et al (2019) Ultrahigh recovery of fracture strength on mismatched fractured amorphous surfaces of silicon carbide. ACS Nano 13:7483–7492

Kim S, Konar A, Hwang WS et al (2012) High-mobility and low-power thin-film transistors based on multilayer MoS_2 crystals. Nat Commun 3:1011

Kim TY, Amani M, Ahn GH et al (2016) Electrical properties of synthesized large-area MoS_2 field-effect transistors fabricated with inkjet-printed contacts. ACS Nano 10:2819–2826

Lee DH, Song D, Kang YS et al (2015) Three-dimensional monolayer graphene and TiO_2 hybrid architectures for high-efficiency electrochemical photovoltaic cells. J Phys Chem C 119:6880–6885

Li J, Naiini MM, Vaziri S et al (2014) Inkjet printing of MoS_2. Adv Func Mater 24:6524–6531

Li D, Wang X, Zhang Q et al (2015a) Nonvolatile floating-gate memories based on stacked black phosphorus-boron nitride-MoS_2 heterostructures. Adv Func Mater 25:7360–7365

Li Q, Chen L, Gadinski MR et al (2015b) Flexible high-temperature dielectric materials from polymer nanocomposites. Nature 523:576–579

Li Z, Xie D, Dai R et al (2016) High-performance heterogeneous complementary inverters based on n-channel MoS_2 and p-channel SWCNT transistors. Nano Res 10:276–283

Lim YR, Han JK, Kim SK et al (2018) Roll-to-roll production of layer-controlled molybdenum disulfide: a platform for 2D semiconductor-based industrial applications. Adv Mater 30:1705270

Liu W, Sarkar D, Kang J et al (2015) Impact of contact on the operation and performance of back-gated monolayer MoS_2 field-effect-transistors. ACS Nano 9:7904–7912

Miyoshi M, Mizuno M, Arima Y et al (2015) Transfer-free graphene synthesis on sapphire by catalyst metal agglomeration technique and demonstration of top-gate field-effect transistors. Appl Phys Lett 107:073102

Shih C-J, Wang QH, Son Y et al (2014) Tuning on-off current ratio and field-effect mobility in a MoS_2 graphene heterostructure via Schottky barrier modulation. ACS Nano 8(6):5790–5798

Shin JH, Kim SH, Kwon SS et al (2018) Direct CVD growth of graphene on three-dimensionally-shaped dielectric substrates. Carbon 129:785–789

Shokouh SHH, Jeon PJ, Pezeshki A et al (2015) High-performance, air-stable, top-gate, p-channel WSe_2 field-effect transistor with fluoropolymer buffer layer. Adv Func Mater 25:7208–7214

Yao Y, Tolentino L, Yang Z et al (2013) High-concentration aqueous dispersions of MoS_2. Adv Func Mater 23:3577–3583

Zhang Z, Wang Bo, Kang R et al (2015) Changes in surface layer of silicon wafers from diamond scratching. CIRP Ann Manuf Technol 64:349–352

Zhang Z, Yuefeng Du, Huang S et al (2020) Macroscale superlubricity: macroscale superlubricity enabled by graphene-coated surfaces. Adv Sci 7:1903239

Zhenyu Z, Fengwei H, Xianzhong Z et al (2012a) Fabrication and size prediction of crystalline nanoparticles of silicon induced by nanogrinding with ultrafine diamond grits. Scripta Mater 67(7–8):657–660

Zhenyu Z, Yaxing S, Chaoge X et al (2012b) A novel model for undeformed nanometer chips of soft-brittle HgCdTe films induced by ultrafine diamond grits. Scripta Mater 67(2):197–200

Zhenyu Z, Dongming G, Bo W et al (2015) A novel approach of high speed scratching on silicon wafers at nanoscale depths of cut. Sci Rep 5:16395

Zhenyu Z, Junfeng C, Bo W et al (2017) A novel approach of mechanical chemical grinding. J Alloy Compd 726:514–524

Zhenyu Z, Zhifeng S, Yuefeng D et al (2018) A novel approach of chemical mechanical polishing for a titanium alloy using an environment-friendly slurry. Appl Surf Sci 427:409–415

Zhenyu Z, Longxing L, Xinze W et al (2020) Development of a novel chemical mechanical polishing slurry and its polishing mechanisms on a nickel alloy. Appl Surf Sci 506:144670

ZhenYu Z, YanXia H, Dongming G et al (2013) A model for nanogrinding based on direct evidence of ground chips of silicon wafers. Sci China Technol Sci 56(9):2099–2108

Ziyu L, Yan W, Chen Z et al (2018) Photo-tunable biomemory based on light-mediated charge trap. Adv Sci 5:1800714

Ziyu L, Chen M, Qian F et al (2019) Mimicking neuroplasticity in a hybrid biopolymer transistor by dual modes modulation. Adv Funct Mater 29:1902374

Ziyu L, Yan W, Jingrui C et al (2020) Semiconductor quantum dots for memories and neuromorphic computing systems. Chem Rev 10:9b00730